Single-chip Type with Built-in FET Switching Regulators

Flexible Step-down Switching Regulator with Built-in Power MOSFET

BD9673EFJ

No.11027EBT57

●Description

Output 1.5A and below High Efficiency Rate Step-down Switching Regulator Power MOSFET Internal Type BD9673EFJ mainly used as secondary side Power supply, for example from fixed Power supply of 12V, 24V etc, Step-down Output of 1.2V/1.8V/3.3V/5V, etc, can be produced. This IC has external Coil/Capacitor down-sizing through 300 kHz Frequency operation, inside Nch-FET SW for 45V “withstand-pressure” commutation and also, high speed load response through Current Mode Control is a simple external setting phase compensation system, through a wide range external constant, a compact Power supply can be produced easily.

●Features

1) Internal 200 mΩ Nch MOSFET
2) Output Current 1.5A
3) Oscillation Frequency 300kHz
4) Synchronizes to External Clock (200kHz～500kHz)
5) Feedback Voltage 1.0V±1.0%
6) Internal Soft Start Function
7) Internal Over Current Protect Circuit, Low Input Error Prevention Circuit, Heat Protect Circuit
8) ON/OFF Control through EN Pin (Standby Current 0 A Typ.)
9) Package: HTSOP-J8 Package

●Applications

For Household machines in general that have 12V/24V Lines, etc.

●Absolute Maximum Rating

Parameter	Symbol	Ratings	Unit
VCC-GND Supply Voltage	VCC	45	V
BST-GND Voltage	VBST	50	V
BST-Lx Voltage	⊿VBST	7	V
EN-GND Voltage	VEN	45	V
Lx-GND Voltage	VLX	45	V
FB-GND Voltage	VFB	7	V
VC-GND Voltage	VC	7	V
SYNC-GND Voltage	SYNC	7	V
High-side FET Drain Current	IDH	2.0	A
Power Dissipation	Pd	3.76(*1)	W
Operating Temperature	Topr	-40～+105	℃
Storage Temperature	Tstg	-55～+150	℃
Junction Temperature	Tjmax	+150	℃

(*1)During mounting of 70×70×1.6t mm 4layer board (Copper area:70mm×70mm).Reduce by 30.08mW for every 1℃ increase. (Above 25℃)

●Operating Conditions (Ta=25℃)

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	VCC	7	—	42	V
Output Voltage	VOUT	1.0(*2)	—	VCC×0.7	V

(*2)Restricted by minimum on pulse typ. 200ns

●**Electrical Characteristics** (Unless otherwise specified, Ta=25℃,VCC=24V, Vo=5V, EN=3V)

Parameter		Symbol	Limits			Unit	Conditions
			Min.	Typ.	Max.		
【Circuit Current】							
Stand-by current of VCC		Ist	—	0	10	μA	VEN=0V
Circuit current of VCC		Icc	—	1	2	mA	FB=1.2V
【Under Voltage Lock Out (UVLO)】							
Detect Voltage		Vuv	6.1	6.4	6.7	V	
Hysteresis width		Vuvhy	—	200	300	mV	
【Oscillator】							
Oscillating frequency		fosc	270	300	330	kHz	
Max Duty Cycle		Dmax	85	91	97	%	
【Error Amp】							
FB threshold voltage		VFB	0.990	1.000	1.010	V	
Input bias current		IFB	-1.0	0	1.0	μA	VFB=0V
Error amplifier DC gain		A_{VEA}	700	7000	70000	V/V	
Trans Conductance		G_{EA}	110	220	440	μA/V	IVC=±10μA, VC=1.5V
Soft Start Time		Tsoft	7	10	13	ms	
【Current Sense Amp】							
VC to switch current transconductance		G_{CS}	5	10	20	A/V	
【Output】							
Lx NMOS ON resistance		RonH	—	200	340	mΩ	
Lx pre-charge NMOS ON resistance		RonL	—	10	17	Ω	
Over Current Detect Current		Iocp	2.0	3.3	—	A	
【CTL】							
EN Pin Control voltage	ON	VENON	2	—	VCC	V	
	OFF	VENOFF	-0.3	—	0.8	V	
EN Pin input current		REN	2.7	5.5	11	μA	VEN=3V
【SYNC】							
SYNC Pin Control voltage	High	VSYNCH	2.0	—	5.5	V	
	Low	VSYNCL	-0.3	—	0.8	V	
SYNC Pin input current		REN	6	12	24	μA	VSYNC=3V
SYNC falling edge to LX rising edge delay		tdelay	200	400	600	ns	

◎ Not designed to withstand radiation.

●Pin Description

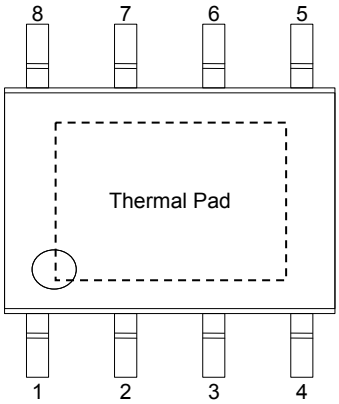


Fig.1 Pin Layout Diagram

Pin No.	Pin Name	Function
1	Lx	Terminal for inductor
2	GND	Ground pin
3	VC	Error amplifier output
4	FB	Inverting node of the trans conductance error amplifier
5	SYNC	Input pin of an external signal for the device synchronized by external signal
6	EN	Stand-by ON/OFF pin
7	BST	Voltage Supply pin for High Side FET Driver
8	VCC	Voltage input pin

●Block Diagram

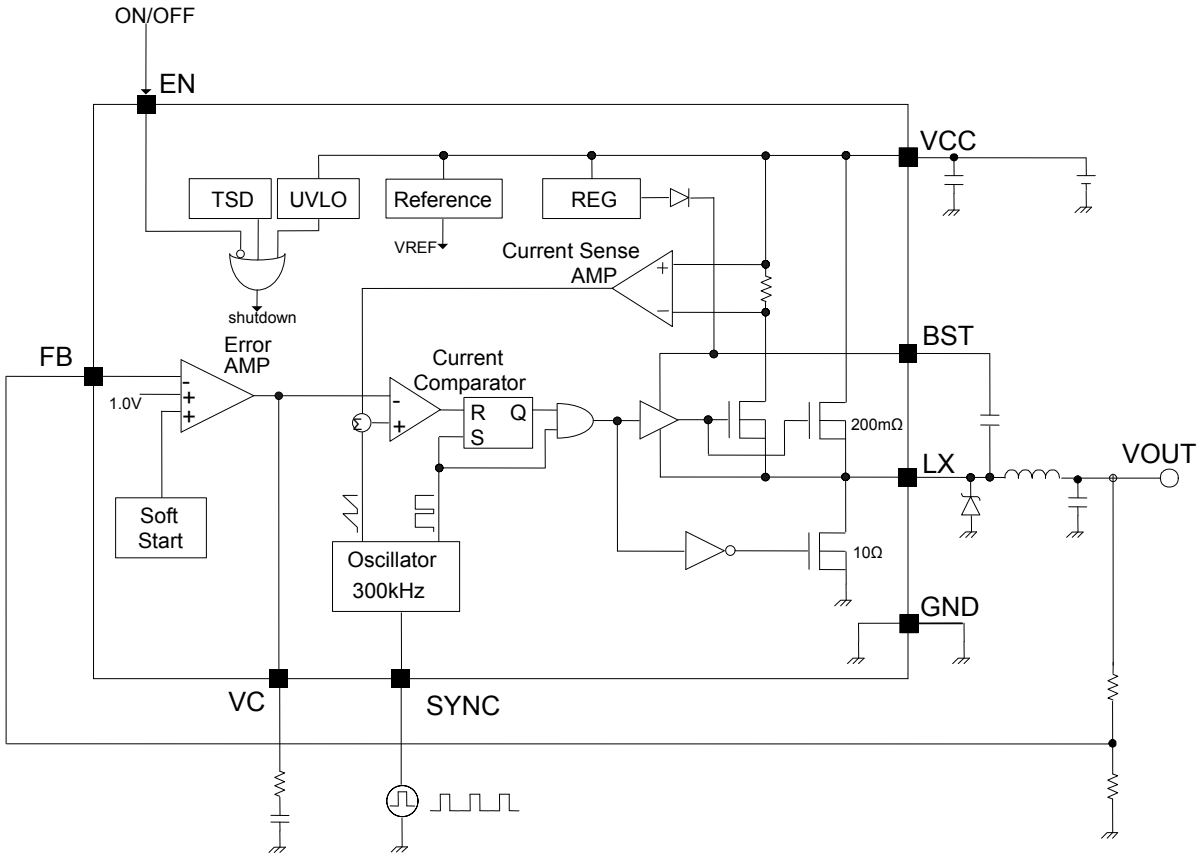


Fig.2 Block Diagram

●Block Description

1. Reference
   This block generates Error Amp standard voltage.
   Standard voltage is 1.0V.

2. REG
   This is a Gate Drive Voltage Generator and 5V Low saturation regulator for internal circuit power supply.

3. OSC
   This is a precise wave oscillation circuit with operation frequency fixed to 300 kHz fixed (self-running mode). To implement the synchronization feature connect a square wave (Hi Level: higher than 2V, Low Level: lower than 0.8V)to the SYNC pin. The synchronization frequency range is 200 kHz to 500 kHz. After connecting the rising edge of LX will be synchronized to the falling edge of SYNC pin signal after 3 counts. At the synchronization remove the external clock, the device transitions self-running mode after 7 microseconds.

4. Soft Start
   A circuit that does soft start to the output voltage of DC/DC comparator, and prevents rush current during start-up. Soft start time is set at IC internal, after 10 ms from starting-up EN pin, standard voltage comes to 1.0V, and output voltage becomes set voltage.

5. ERROR AMP
   This is an Error amplifier what detects output signal, and outputs PWM control signal.
   Internal Standard Voltage is set to 1.0V.
   Also, C and R are connected between the output (VC) pin GND of Error Amp as Phase compensation elements.
   (See p.11)

6. ICOMP
   This is a Voltage-Pulse Width Converter that controls output voltage in response to input voltage.
   This compares the Voltage added to the internal SLOPE waveform in response to the FET WS current with Error amplifier output voltage, controls the width of output Pulse and outputs to driver.

7. Nch FET SW
   This is an internal commutation SW that converts Coil Current of DC/DC Comparator.
   It contains 45V" with stand pressure" 200mΩ SW.
   Because the Current Rating of this FET is 2.0A included ripple current, please use at within 2.0A.
   The device has the circuit of over current protection for protecting the FET from over current.
   To detect OCP 2 times sequentially, the device will stop and after 13msec restart.

8. UVLO
   This is a Low Voltage Error Prevention Circuit.
   This prevents internal circuit error during increase of power supply voltage and during decline of power supply voltage.
   It monitors VCC pin voltage and internal REG voltage, and when VCC voltage becomes 6.4V and below, it turns off all output FET and turns off DC/DC comparator output and soft start circuit resets.
   Now this threshold has hysteresis of 200mV.

9. TSD
   This is a Heat Protect (Temperature Protect) Circuit.
   When it detects an abnormal temperature exceeding Maximum Junction Temperature (Tj=150℃), it turns off all output FET, and turns off DC/DC comparator output. When Temperature falls, it has/with hysteresis and automatically returns.

10. EN
    With the Voltage applied to EN Pin (6pin), IC ON/OFF can be controlled.
    When a Voltage of 2.0V or more is applied, it turns on, at open or 0V application, it turns off.
    About 550 kΩ pull-down resistance is contained within the pin.

●Detailed Description

◇Synchronizes to External Clock

The SYNC pin can be used to synchronize the regulator to an external system clock. To implement the synchronization feature connect a square wave to SYNC pin. The square wave amplitude must transition lower than 0.8V and higher than 2.0V on the SYNC pin and have an on time greater than 100 ns and an off time greater than 100 ns. The synchronization frequency range is 200 kHz to 500 kHz. The rising edge of the LX will be synchronized to the falling edge of SYNC pin signal after SYNC input pulse 3 count. At the synchronization, the external clock is removed, the device transitions self-running mode after 7 microseconds.

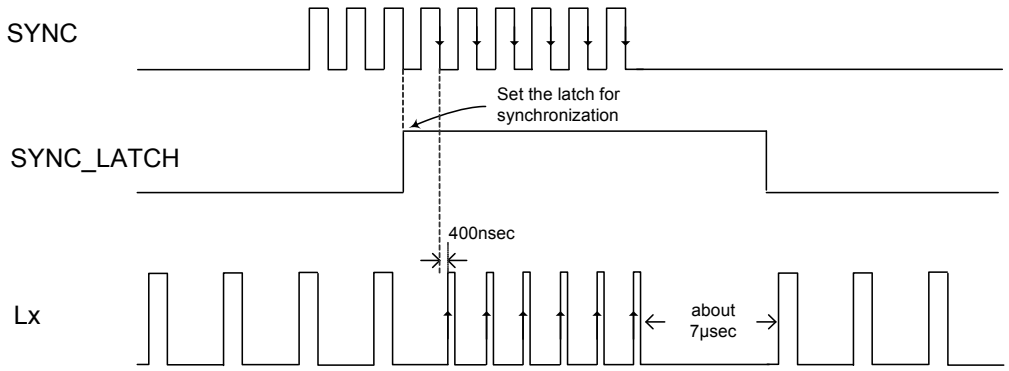


Fig.3 Timing chart at Synchronization

◇SOFT START

The soft start time of BD9763EFJ is determined by the DCDC operating frequency (self-run mode 300 kHz ⇒10ms). If synchronization is used at the time of EN=ON, The soft start time is restricted by SYNC pin input pulse frequency. SYNC pin input pulse frequency is fosc_ex kHz, the soft start time is expressed by below equation.

$$Tss = \frac{300}{fosc\_ex} \times 10\ [ms]$$

◇OCP operation

The device has the circuit of over current protection for protecting the FET from over current. To detect OCP 2 times sequentially, the device will stop and after 13msec restart.

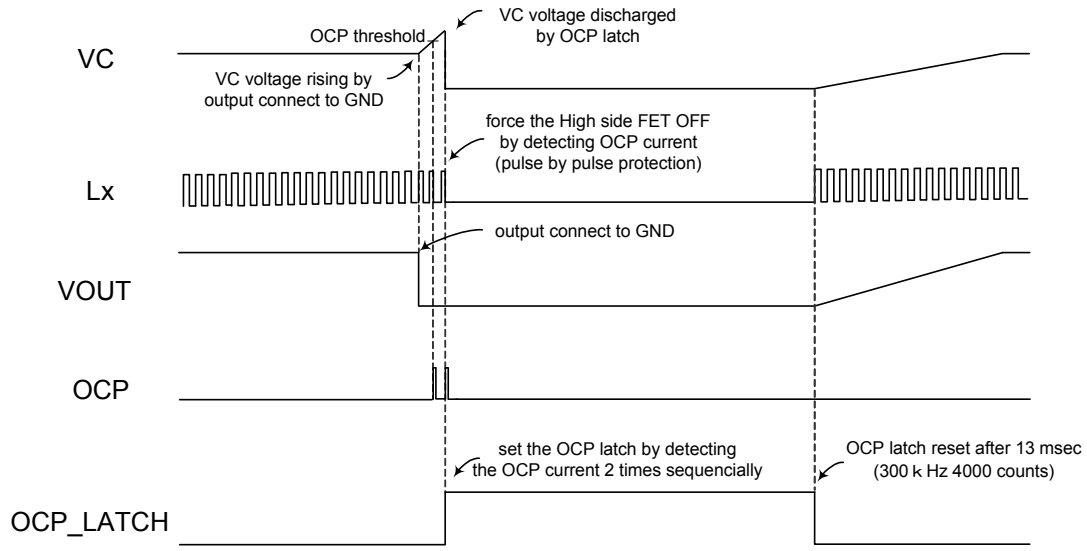


Fig.4 Timing chart at OCP operation

●**Reference Data** (Unless otherwise specified, Ta=25℃,VCC=24V, Vo=5V,EN=3V)

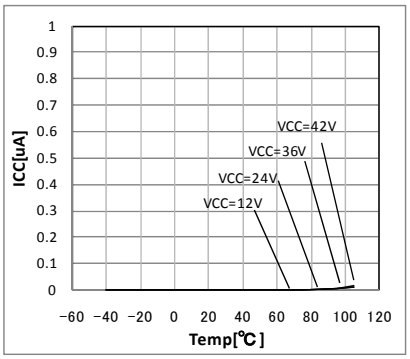


Fig.5. Standby Current
Temperature Characteristics

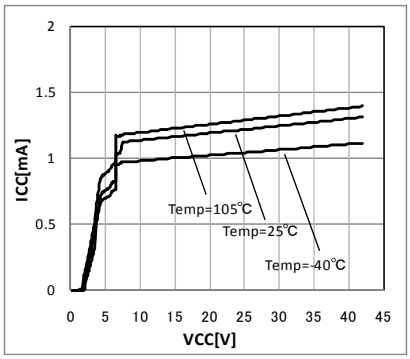


Fig.6. Circuit Current
Power supply Voltage Characteristics

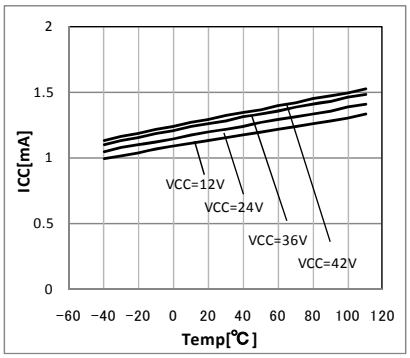


Fig.7. Circuit Current
Temperature Characteristics

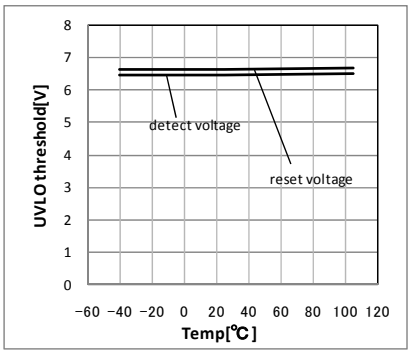


Fig.8. UVLO Threshold
Temperature Characteristics

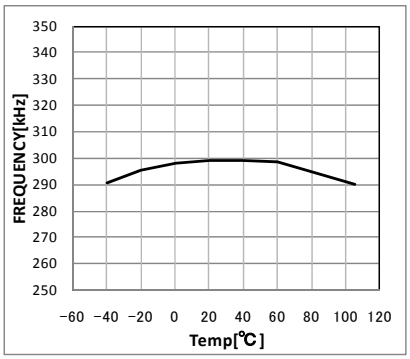


Fig.9. Oscillation Frequency
Temperature Characteristics

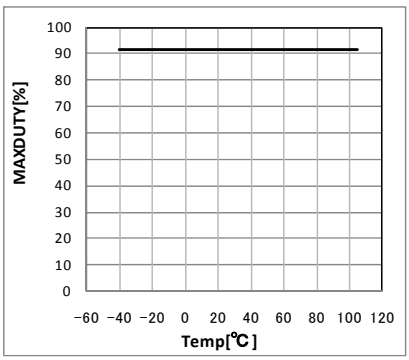


Fig.10. Max Duty Temperature
Characteristics

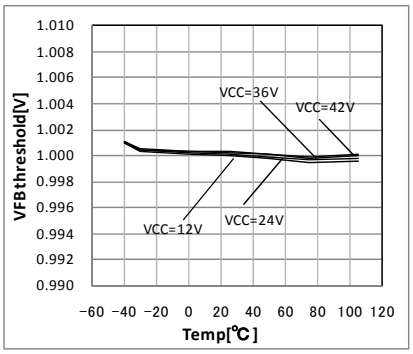


Fig.11. FB Threshold Voltage
Temperature Characteristics

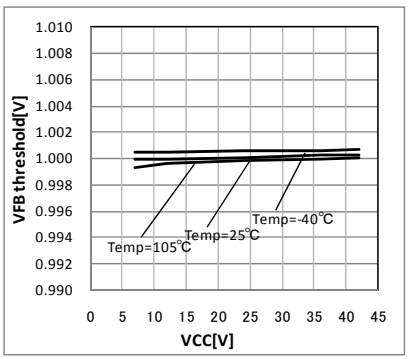


Fig.12. FB Threshold Power
supply Characteristics

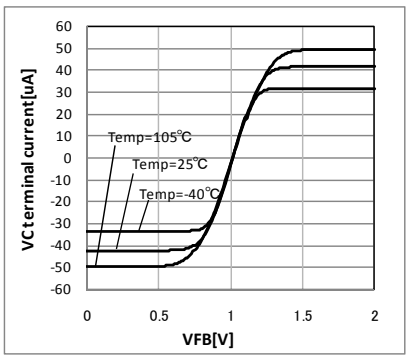


Fig.13. FB Voltage －VC
Current Characteristics

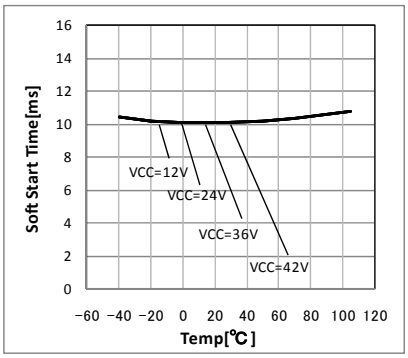


Fig.14. Soft Start Time Temperature Characteristics

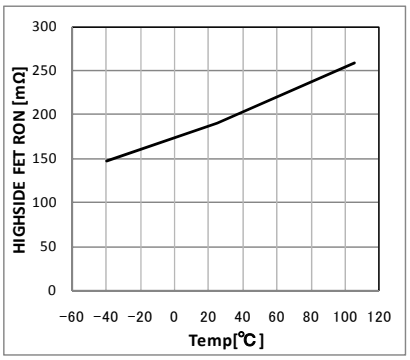


Fig.15. Nch FET ON Resistance Temperature Characteristics

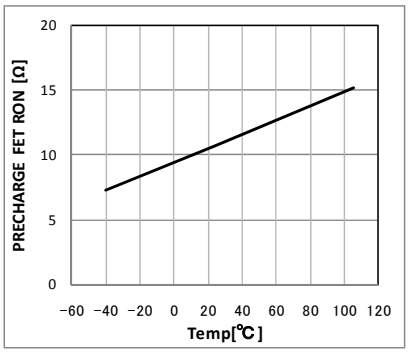


Fig.16. Pre-charge FET ON Resistance Temperature Characteristics

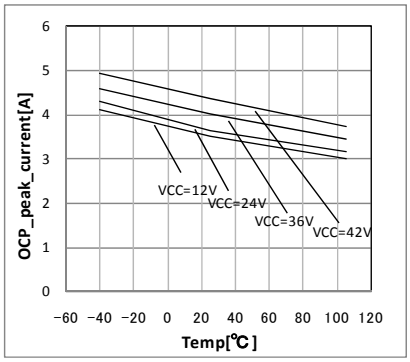


Fig.17. OCP Detect Current Temperature Characteristics

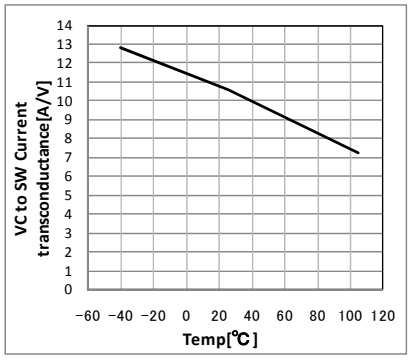


Fig.18. VC to SW current transconductance Temperature characteristics

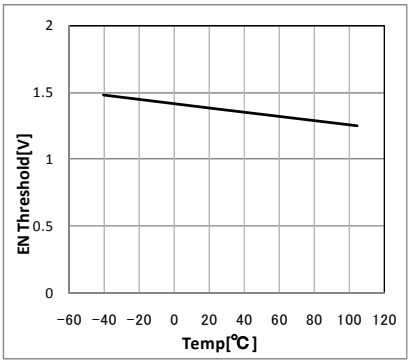


Fig.19. EN Threshold Temperature Characteristics

●Example of Reference Application Circuit (Input 24V, Output 5.0V/ 1A)

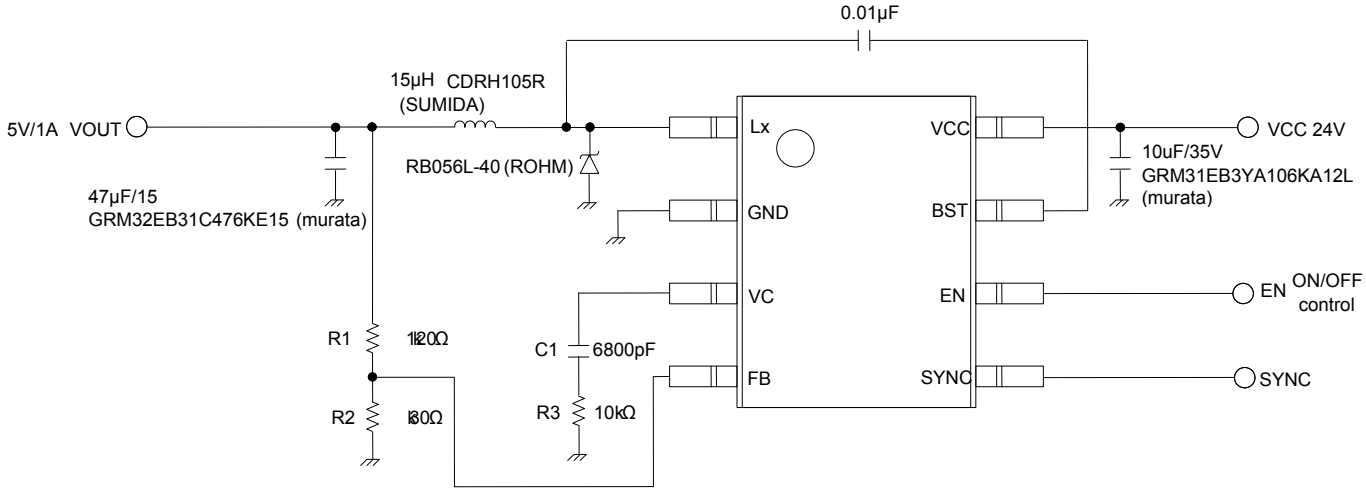


Fig.20 Reference Application Circuit

●Reference Application Data (Example of Reference Application Circuit)

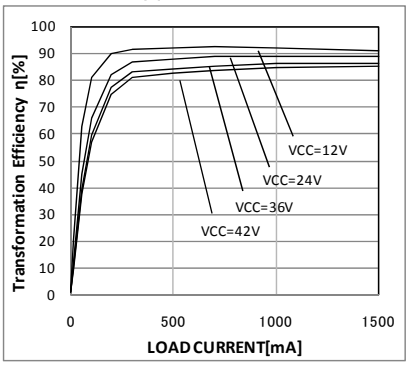


Fig.21 Electric Power Conversion Rate

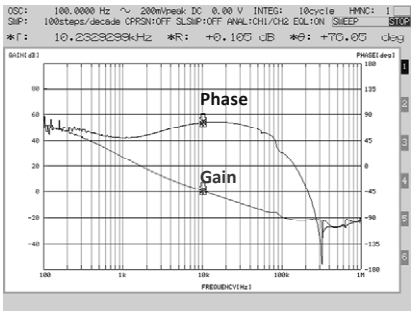


Fig.22 Frequency Response Characteristics(Io=0.5A)

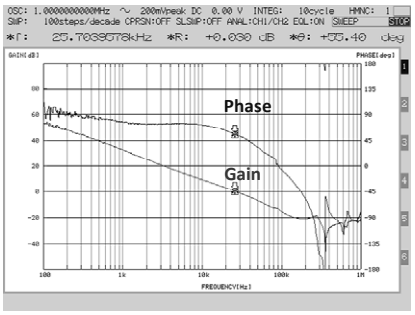


Fig.23 Frequency Response Characteristics (Io=1.0A)

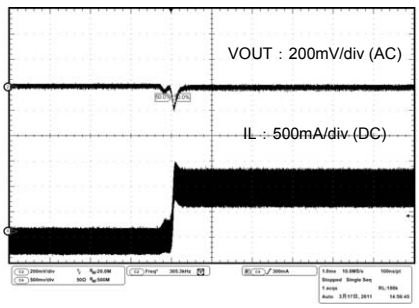


Fig.24 Load Response Characteristics (Io=0A→1.5A)

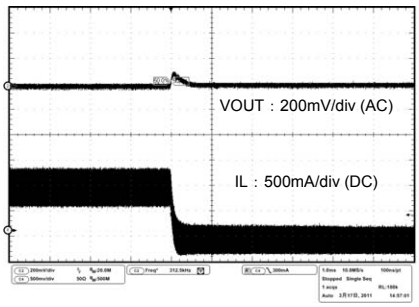


Fig.25 Load Response Characteristics (Io=1.5A→0A)

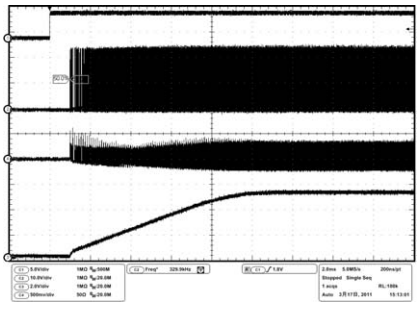


Fig.26 startup Waveform

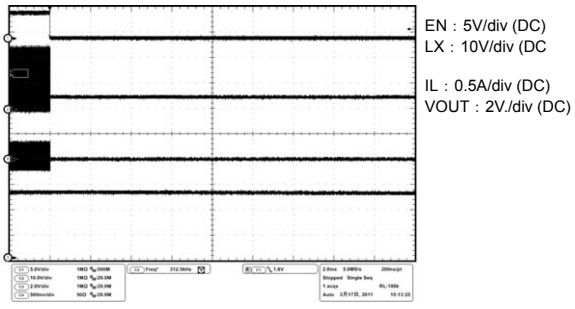


Fig.27 Stop Waveform

●Evaluation Board Layout

Layout is a critical portion of good power supply design. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VCC pin should be bypassed to ground with a low ESR ceramic bypass capacitor with B dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VCC pin, and the anode of the catch diode. See Fig.28 for a PCB layout example. The GND pin should be tied directly to the thermal pad under the IC and the thermal pad.

The thermal pad should be connected to any internal PCB ground planes using multiple VIAs directly under the IC. The LX pin should be routed to the cathode of the catch diode and to the output inductor. Since the LX connection is the switching node, the catch diode and output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts; however this layout has been shown to produce good results and is meant as a guideline.

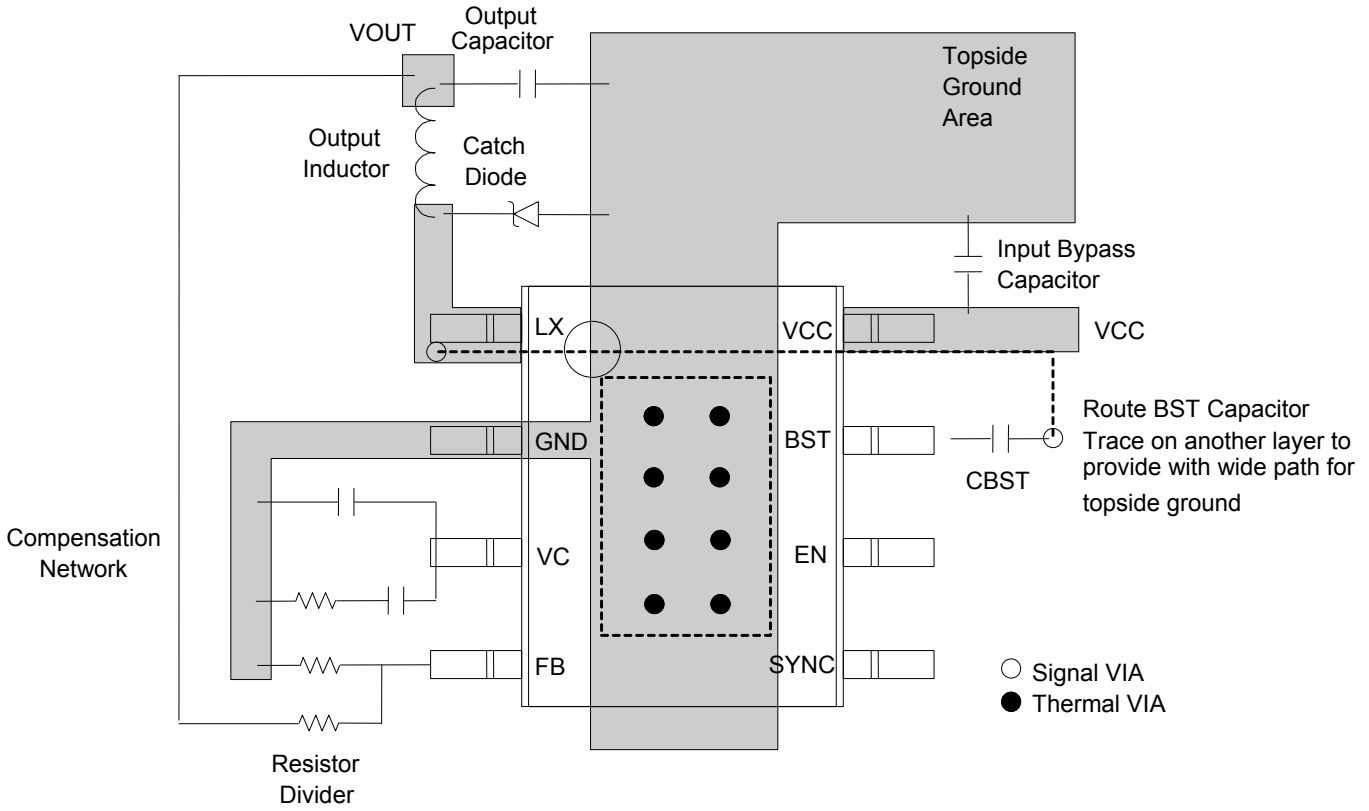


Fig.28 Evaluation Board Pattern

●Application Components Selection Method

(1) Inductor

Something of the shield Type that Fulfills the Current Rating (Current value Ipecac below), with low DCR (Direct Current Resistance element) is recommended. Value of Inductor influences Inductor Ripple Current and becomes the cause of Output Ripple. In the same way as the formula below, this Ripple Current can be made small for as big as the L value of Coil or as high as the Switching Frequency.

$$Ipeak = Iout + \Delta IL/2 \ [A] \quad (1)$$

$$\Delta IL = \frac{Vin-Vout}{L} \times \frac{Vout}{Vin} \times \frac{1}{f} \ [A] \quad (2)$$

(η:Efficiency, ⊿IL:Output Ripple Current, f:Switching Frequency)

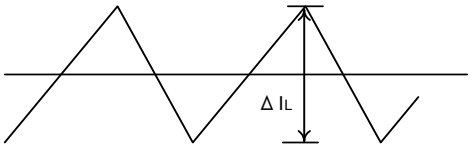


Fig.29 Inductor Current

For design value of Inductor Ripple Current, please carry out design tentatively with about 20%～50% of Maximum Input Current.

※When current that exceeds Coil rating flows to the coil, the Coil causes a Magnetic Saturation, and there are cases wherein a decline in efficiency, oscillation of output happens. Please have sufficient margin and select so that Peak Current does not exceed Rating Current of Coil.

(2) Output Capacitor

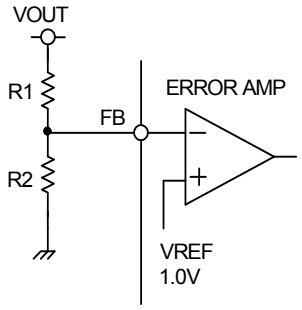
In order for Capacitor to be used in Output to reduce Output Ripple, Low Ceramic Capacitor of ESR is recommended. Also, for Capacitor Rating, on top of putting into consideration DC Bias Characteristics, please use something whose Maximum Rating has sufficient margin with respect to the Output Voltage.
Output Ripple Voltage is looked for using the following formula.

$$Vpp = \Delta IL \times \frac{1}{2\pi \times f \times Co} + \Delta IL \times R_{ESR} \ [V] \quad \cdots \ (3)$$

Please design in a way that it is held within Capacity Ripple Voltage.

(3) Output Voltage Setting

ERROR AMP internal Standard Voltage is 1.0V. Output Voltage is determined as seen in (4) formula.



$$Vo = \frac{(R1+R2)}{R2} \times 1.0 \ [V] \quad \cdots \ (4)$$

Fig.30 Voltage Return Resistance Setting Method

(4) Boost Capacitor

Please connect CBST=0.01μF (Laminate Ceramic Capacitor) between BST Pin-Lx Pins as Output capacitors of Gate Drive Voltage Generator REG (5V).

(5) About Adjustment of DC/DC Comparator Frequency Characteristics
Role of Phase compensation element CC1, CC2, RC (See P.7 Example of Reference Application Circuit)

Stability and Responsiveness of Loop are controlled through VC Pin which is the output of Error Amp.
The combination of zero and pole that determines Stability and Responsiveness is adjusted by the combination of resistor and capacitor that are connected in series to the VC Pin.

DC Gain of Voltage Return Loop can be calculated for using the following formula.

$$Adc = Rl \times Gcs \times A_{EA} \times \frac{V_{FB}}{Vout}$$

Here, VFB is Feedback Voltage (1.0V).A_{EA} is Voltage Gain of Error amplifier (typ : 77dB), Gcs is the Trans-conductance of Current Detect (typ : 10A/V), and Rl is the Output Load Resistance value.

There are 2 important poles in the Control Loop of this DC/DC.
The first occurs with/ through the output resistance of Phase compensation Capacitor (C1) and Error amplifier.
The other one occurs with/through the Output Capacitor and Load Resistor.
These poles appear in the frequency written below.

$$fp1 = \frac{G_{EA}}{2\pi \times C1 \times A_{EA}}$$

$$fp2 = \frac{1}{2\pi \times COUT \times Rl}$$

Here, G_{EA} is the trans-conductance of Error amplifier(typ : 220μA/V).

Here, in this Control Loop, one zero becomes important.
With the zero which occurs because of Phase compensation Capacitor C1 and Phase compensation Resistor R3, the Frequency below appears.

$$fz1 = \frac{1}{2\pi \times C1 \times R3}$$

Also, if Output Capacitor is big, and that ESR (RESR) is big, in this Control Loop, there are cases when it has an important, separate zero (ESR zero).
This ESR zero occurs due to ESR of Output Capacitor and Capacitance, and exists in the Frequency below.

$$fz = \frac{1}{2\pi \times COUT \times RESR}$$

(ESR zero)

In this case, the 3rd pole determined with the 2nd Phase compensation Capacitor (C2) and Phase Correction Resistor (R3) is used in order to correct the ESR zero results in Loop Gain.
This pole exists in the frequency shown below.

$$fp3 = \frac{1}{2\pi \times C2 \times R3}$$

(pole that corrects ESR zero)

The target of Phase compensation design is to create a communication function in order to acquire necessary band and Phase margin.

Cross-over Frequency (band) at which Loop gain of Return Loop becomes “0” is important.
When Cross-over Frequency becomes low, Power supply Fluctuation Response, Load Response, etc worsens.
On the other hand, when Cross-over Frequency is too high, instability of the Loop can occur.
Tentatively, Cross-over Frequency is targeted to be made 1/20 or below of Switching Frequency.

Selection method of Phase Compensation constant is shown below.

1. Phase Compensation Resistor (R3) is selected in order to set to the desired Cross-over Frequency.
   Calculation of RC is done using the formula below.

$$R3 = \frac{2\pi \times COUT \times fc}{G_{EA} \times G_{CS}} \times \frac{Vout}{VFB}$$

   Here, fc is the desired Cross-over Frequency. It is made about 1/20 and below of the Normal Switching Frequency (fs).

2. Phase compensation Capacitor (C1) is selected in order to achieve the desired phase margin.
   In an application that has a representative Inductance value (about several μH～20μH), by matching zero of compensation to 1/4 and below of the Cross-over Frequency, sufficient Phase margin can be acquired. C1 can be calculated using the following formula.

$$C1 > \frac{4}{2\pi \times R3 \times fc}$$

   RC is Phase compensation Resistor.

3. Examination whether the second Phase compensation Capacitor C2 is necessary or not is done.
   If the ESR zero of Output Capacitor exists in a place that is smaller than half of the Switching Frequency, a second Phase compensation Capacitor is necessary. In other words, it is the case wherein the formula below happens.

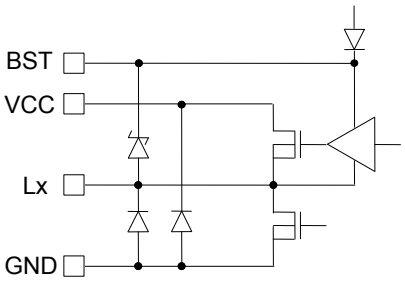
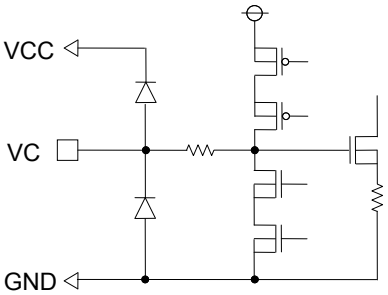
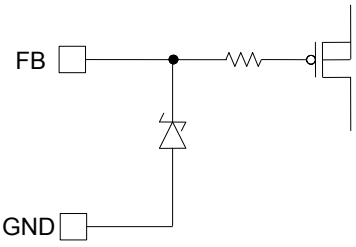
$$\frac{1}{2\pi \times COUT \times RESR} < \frac{fs}{2}$$

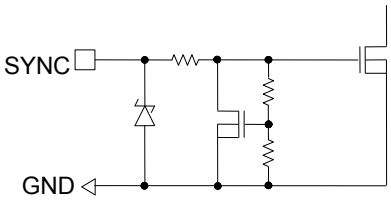
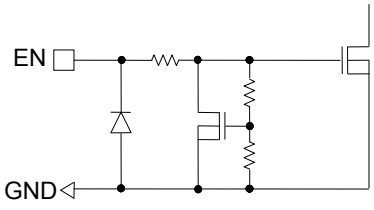
   In this case, add the second Phase compensation Capacitor C2, and match the frequency of the third pole to the Frequency fp3 of ESR zero.

   C2 is looked for using the following formula.

$$C2 = \frac{COUT \times RESR}{R3}$$

●I/O Equivalent Schematic

Pin. No	Pin. Name	Pin Equivalent Schematic
1 2 7 8	Lx GND BST VCC	
3	VC	
4	FB	

Pin. No	Pin. Name	Pin Equivalent Schematic
5	SYNC	
6	EN	

●Notes for use

(1) About Absolute Maximum Rating
When the absolute maximum ratings of application voltage, operating temperature range, etc. was exceeded, there is possibility of deterioration and destruction. Also, the short Mode or open mode, etc. destruction condition cannot be assumed. When the special mode where absolute maximum rating is exceeded is assumed, please give consideration to the physical safety countermeasure for the fuse, etc.

(2) About GND Electric Potential
In every state, please make the electric potential of GND Pin into the minimum electrical potential. Also, include the actual excessive effect, and please do it such that the pins, excluding the GND Pin do not become the voltage below GND.

(3) About Heat Design
Consider the Power Dissipation (Pd) in actual state of use, and please make Heat Design with sufficient margin.

(4) About short circuit between pins and erroneous mounting
When installing to set board, please be mindful of the direction of the IC, phase difference, etc. If it is not installed correctly, there is a chance that the IC will be destroyed. Also, if a foreign object enters the middle of output, the middle of output and power supply GND, etc., even for the case where it is shorted, there is a change of destruction.

(5) About the operation inside a strong electro-magnetic field
When using inside a strong electro-magnetic field, there is a possibility of error, so please be careful.

(6) Temperature Protect Circuit (TSD Circuit)
Temperature Protect Circuit (TSD Circuit) is built-in in this IC. As for the Temperature Protect Circuit (TSD Circuit), because it a circuit that aims to block the IC from insistent careless runs, it is not aimed for protection and guarantee of IC. Therefore, please do not assume the continuing use after operation of this circuit and the Temperature Protect Circuit operation.

(7) About checking with Set boards
When doing examination with the set board, during connection of capacitor to the pin that has low impedance, there is a possibility of stress in the IC, so for every 1 process, please make sure to do electric discharge. As a countermeasure for static electricity, in the process of assembly, do grounding, and when transporting or storing please be careful. Also, when doing connection to the jig in the examination process, please make sure to turn off the power supply, then connect. After that, turn off the power supply then take it off.

(8) About common impedance
For the power supply and the wire of GND, lower the common impedance, then, as much as possible, make the ripple smaller (as much as possible make the wire thick and short, and lower the ripple from L・C), etc., then and please consider it sufficiently.

(9) In the application, when the mode where the VCC and each pin electrical potential becomes reversed exists, there is a possibility that the internal circuit will become damaged. For example, during cases wherein the condition when charge was given in the external capacitor, and the VCC was shorted to GND, it is recommended to insert the bypass diode to the diode of the back current prevention in the VCC series or the middle of each Pin-VCC.

(10) About High-side Nch FET
Please use within 2.0A contained ripple current, because the absolute maximum rating of high-side Nch FET is 2.0A.

(11) About over current detection
The detecting current is the current flowing through high-side NchFET. Output current containing ripple current, therefore the detecting current is the current of the output current containing ripple current.

(12) About IC Pin Input

This IC is a Monolithic IC, and between each element, it has P^+ isolation for element separation and P board. With the N layer of each element and this, the P-N junction is formed, and the parasitic element of each type is composed.
For example, like the diagram below, when resistor and transistor is connected to Pin,

○When GND＞(PinA) in Resistor, when GND＞(PinA), when GND＞(Pin B) in Transistor (NPN), the P-N junction will operate as a parasitic diode.

○Also, during GND＞(Pin B) in the Transistor (NPN), through the N layer of the other elements connected to the above-mentioned parasitic diode , the parasitic NPN Transistor will operation.

On the composition of IC, depending on the electrical potential, the parasitic element will become necessary. Through the operation of the parasitic element interference of circuit operation will arouse, and error, therefore destruction can be caused. Therefore please be careful about the applying of voltage lower than the GND (P board) in I/O Pin, and the way of using when parasitic element operating.

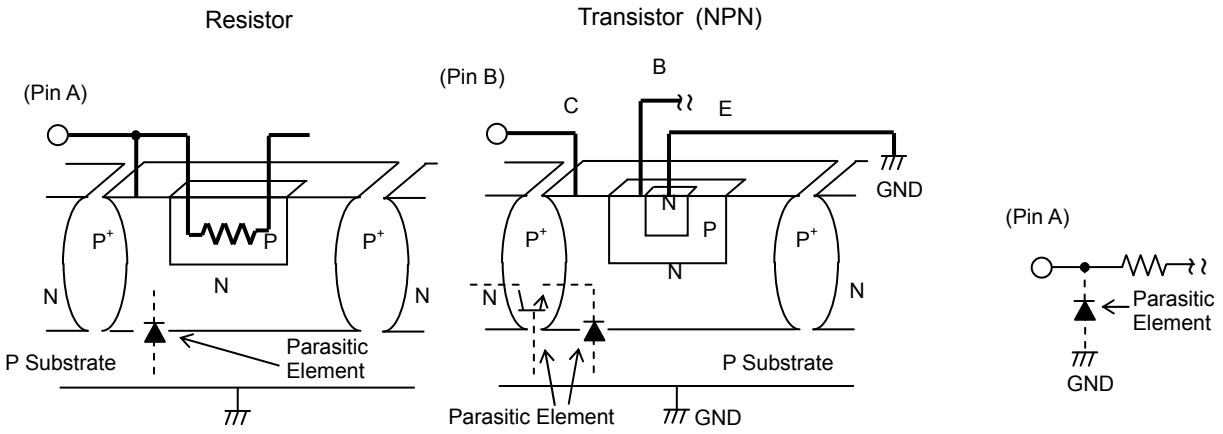


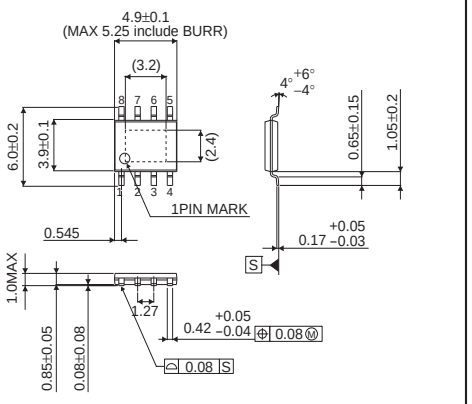
Fig.31 Example of simple structure of Bipolar IC

●Ordering part number

B	D	9	6	7	3	E	F	J	-	E	2

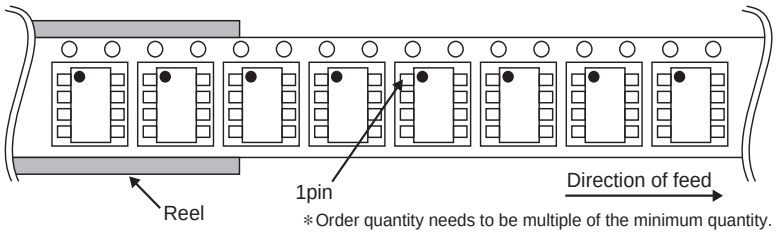
Part No. Part No. Package EFJ : HTSOP-J8 Packaging and forming specification E2: Embossed tape and reel

HTSOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



＊Order quantity needs to be multiple of the minimum quantity.

Notes

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